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# FPGA based Image Feature Extraction Using Xilinx System Generator

Swapnil G. Kavitkar
*Electronics and Telecommunication Engineering*

Prashant L. Paikrao
*Electronics and Telecommunication Engineering*

***Abstract*— Image Features are the basis for most of the real time image processing applications. Edge is one of the prime features of image. It helps us to analyze, infer and take decision in various image processing applications. In this paper sobel and prewitts algorithms are implemented over Field Programmable Gate Array (FPGA). Real time system demands dedicated hardware for image processing. Prototype of the ASIC can be obtained by FPGA based implementation of edge detection algorithm. FPGA has many significant features, that serves as a platform for processing real time algorithm. It gives substantially higher performance over programmable Digital Signal Processor (DSPs) and microprocessor. Modern approach of 'Xilinx System Generator' (XSG) is used for system modeling and FPGA programming. XSG is a tool of matlab that generates bit stream file (*.bit), netlist, timing and power analysis.**

***Keywords- Image features, FPGA, XSG, Matlab.***

## I. INTRODUCTION

Image processing improves the subjective quality of image. Low level image processing operations like image segmentation using edge detection and feature extraction helps us to analyze, infer and take decision in various applications. It focuses on processing an image pixel by pixel and over its neighborhood. Feature extraction algorithms are essential for many computer vision applications such as object recognition, real time flaw detection, meteorological applications, image target area identification, region formation, etc.

Edge detection outlines the points in images correspond to sharp intensity variations or discontinuities. The discontinuities are abrupt variations in pixels intensity which characterize boundaries of objects in a scene structure. Sobel edge detection algorithm is widely used feature extraction algorithm owing to its reliable performance under different circumstances.

FPGA is 'fine grained device' with high-speed parallel computing capacity. It is rich source of high speed multipliers, adder, and memory; it offers relative ease of implementation of complex convolution. FPGA based design offer an advantage of short Turn Around Time (TAT) and small Non Recurrent Expense (NRE). Instead of traditional approach of hardware implementation Xilinx introduces novice and advance approach of hardware implementation 'Xilinx System Generator' of Xilinx. By eradicating the complicated simulation comparison and verification processes, it speed up the FPGA based system. The platform integrates design entry, logic synthesis, place and route.

## II. EXISTING SYSTEM

An extensive work is done in the field feature extraction for real time image processing. Edge detection being fundamental step for any image processing operation, it provokes great interest in research fraternity. Edge detection alters the image for human interpretation and information extraction; It is useful in various fields such as in biomedical applications, satellite imaging, traffic control, land acquisition, etc.

Literature reveals that hardware implementation of edge detection algorithm is necessary to meet real time and speed constraints. In [2] high throughput rate is achieved for FPGA based implementation of canny edge detection algorithm exploiting the FPGA resource at its peak. FPGA based object detection using edge information is [3] proposed to offer high speed, energy efficient design. Simplified approach for hardware implementation using 'Xilinx System Generator' is proposed in [4] for vehicle edge detection for traffic analysis. Comparative analysis for software and hardware based video image edge detection is proposed [5] hardware implementation tends to yield faster results. Machine implementation and analysis of pattern is proposed using canny edge detector algorithm in [6] satisfactory results are obtained. Sobel edge detection algorithm is implemented [7] over hardware platform for optimized volume. Hardware co-simulation for video edge detection is implemented over Xilinx Virtex 5 board in [8] using XSG. Real time FPGA based tracking and counting system for people is proposed in [9] Spartan 3E is used as hardware platform.

### 1. Edge detection

The edge is characterized by its length, slope angle and coordinate of the slope midpoint. Edges are caused by variety of factors such as surface normal discontinuity, depth discontinuity, surface color discontinuity, illumination discontinuity. Basically there are two types of edges a ramp edge, where the intensity values change slowly and a step edge or an ideal edge, where the intensity values change abruptly.

Edge detection can be achieved by several approaches, the majority may be grouped into two categories, Gradient (Approximation of derivative) and Laplacian (Zero crossing detectors) based approach. For edge detection original image is to be convolved with coefficient of gradient of high pass filter obtained along **x** and **y** direction.

Results are added together which yields edges in an images. This can be mathematically formulated as

$$|G|=|Gx|+|Gy| \quad (1)$$

Mathematically gradient can be computed with equation.

$$|G| = \sqrt{Gx^2 + Gy^2} \quad (2)$$

Edge detection algorithms are classified on the basis of arrangement of coefficient of gradient operators.

## 2. Edge detection algorithms

Several edge detection algorithms are available broadly they are classified into first order derivative (gradient) and second order derivative (laplacian) based approach [10][11]. First order derivative includes Robert operator, sobel operator, prewitt operator, compass operator, canny edge detection operator. Second order derivative is classified as Laplacian operator, Zero crossing evaluation, Hough transform, etc.

### A. Prewitts edge detection algorithm

Robert mask used prior to Prewitt operator for edge is even size mask hence; It has limitation when used for implementation of algorithm. This problem is completely eliminated in Prewitts operator, named after inventor. In this algorithm while approximating the first derivative similar weights are assigned to all the neighborhood candidate pixel whose edge strength is calculated. Prewitts operator has faster computational speed. Kernel can be designed based on mathematical equation.

$$|\nabla Z| = |(I_7 + I_8 + I_9) - (I_1 + I_2 + I_3)| + |(I_3 + I_6 + I_9) - (I_1 + I_4 + I_7)| \quad (4)$$

Where, I is coefficient of gradient operator. And $|\nabla Z|$ is a gradient operator . Convolution mask for edge detection using prewitt operator is given as shown in Fig.1 given below

| | | |
|---|---|---|
| -1 | 0 | +1 |
| -1 | 0 | +1 |
| -1 | 0 | +1 |

Gx

| | | |
|---|---|---|
| +1 | +1 | +1 |
| 0 | 0 | 0 |
| -1 | -1 | -1 |

Gy

Fig.1: Convolution mask of edge detection (Prewitt)

### C. Sobel edge detection algorithm

It addresses limitation of Robert edge detection algorithm and confer better performance over prewitt operator. In sobel algorithm higher weights are assigned to the pixels close to the candidate pixel. The Sobel operator is first order edge detection operator, It computes gradient of the image as intensity function. The Sobel operator only considers the two orientations which are 0 and 90 degrees as convolution kernels. Absolute magnitude of the gradient at each point of image can be obtained by merging Kernels together. Kernels can be designed on the basis of mathematical equations computing gradient values is given below.

$$|\nabla Z| = |(I_7 + 2I_8 + I_9) - (I_1 + 2I_2 + I_3)| + |(I_3 + 2I_6 + I_9) - (I_1 + 2I_4 + I_7)| \quad (5)$$

Where, I is coefficient of gradient operator. And $|\nabla Z|$ is a gradient operator. Convolution mask is given in Fig.2

| | | |
|---|---|---|
| -1 | 0 | +1 |
| -2 | 0 | +2 |
| -1 | 0 | +1 |

Gx

| | | |
|---|---|---|
| +1 | +2 | +1 |
| 0 | 0 | 0 |
| -1 | -2 | -1 |

Gy

Fig.2: Convolution mask of edge detection (Sobel)

## III. Proposed Work

### 1. System flow

Methodology includes designing of edge detection system in matlab using 'Xilinx System Generator' (simulink block). Model generates HDL code and netlist that can be Synthesized and optimized using ISE 13.1. It is implemented over Spartan 3E FPGA. Flow of Xilinx system generator is depicted in fig.2. It finally generates bit stream file that can be loaded into FPGA. Significant drawback of traditional approach used for hardware implementation is that it uses a high level language for coding; finally generating bit stream file. Xilinx introduced the advanced system modeling tool (Xilinx System Generator) that has lucid system development approach [13].

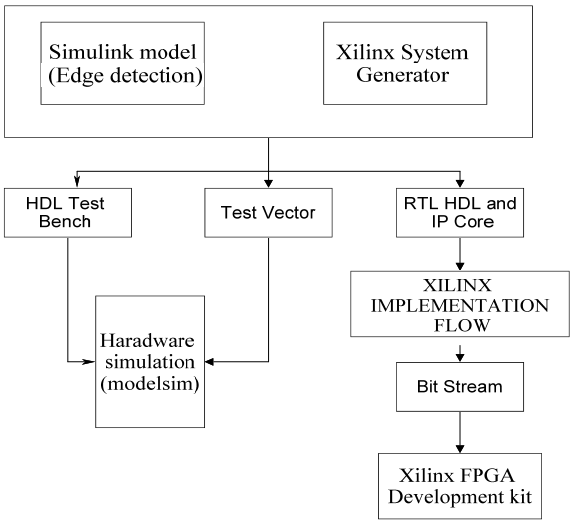


Fig.3: Block diagram for XSG design flow

Flow of the edge detection unit is depicted in Fig.4.It includes image pre-processing and post-processing operations. They make data available in suitable format for processing over FPGA platform. Edge detection unit is nothing but a high pass filter designed using 'Xilinx System Generator'. It is placed between pre-processing and post-processing block.

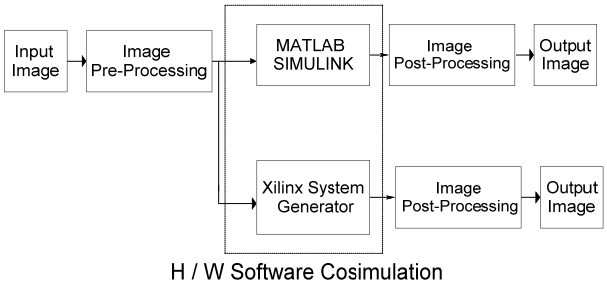


Fig.4: Block diagram for system design.

## 2. System Implementation

In this paper sobel and prewitts edge detection algorithm is implemented over FPGA platform and their comparative analysis is shown. Hardware implementation using XSG is as follow.

### a. Image Pre-processing Block diagram

Image pre-processing is shown in Fig.5. Primary significance of image pre-processing operation is serialization of data with suitable data rate for the hardware implementation.

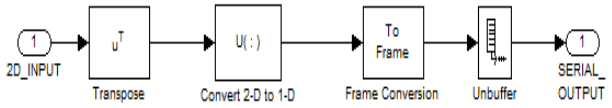


Fig.5: Image Pre-processing block diagram

### b. Image Post-processing Block diagram

Image post-processing is shown in Fig.6. Primary significance of image post-processing is to make processed data available and with suitable data rate for displaying in matlab environment.

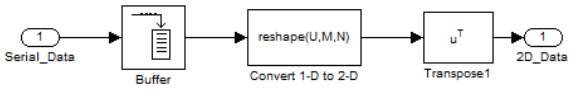


Fig.6: Image Post-processing block diagram

### a. Horizontal Gradient filter for Sobel operator

Horizontal gradient of image is computed by moving horizontal kernel for sobel edge detection over an image.

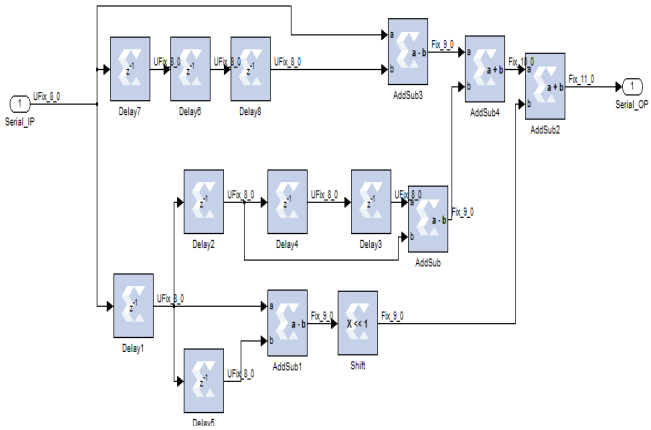


Fig.7: XSG based Horizontal gradient filter (Sobel)

### b. Vertical Gradient filter for Sobel operator

Vertical gradient of image is computed by moving vertical kernel for sobel edge detection over an image.

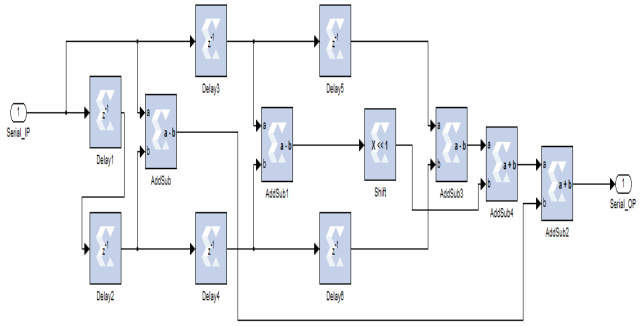


Fig.8: XSG based Vertical gradient filter (Sobel).

### c. Horizontal Gradient filter for Prewitt operator

Horizontal gradient of image is computed by moving horizontal kernel for Prewitt edge detection over an image

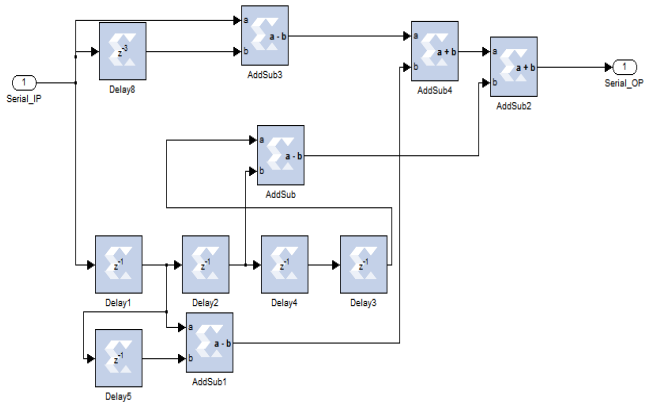


Fig.9: Horizontal gtradient filter (Prewitt).

### d. Vertical Gradient filter for Prewitt operator

Vertical gradient of image is computed by moving vertical mask for Prewitt edge detection over an image

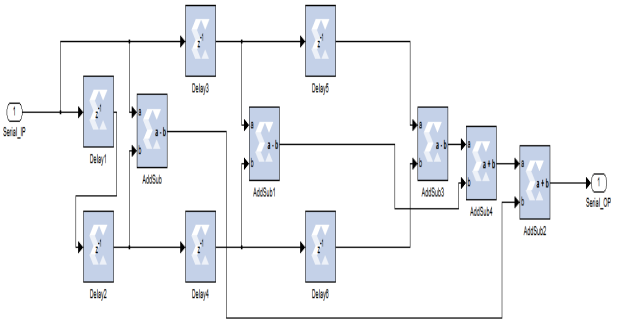


Fig.10: Vertical gradient filter (Prewitt)

## IV. Result And Analysis

The hardware implementation results are produced using Xilinx Spartan-3E FPGA for sobel and prewitt operator. Fig.11 shows edge detection results using Sobel operator for XSG and hardware implementation.

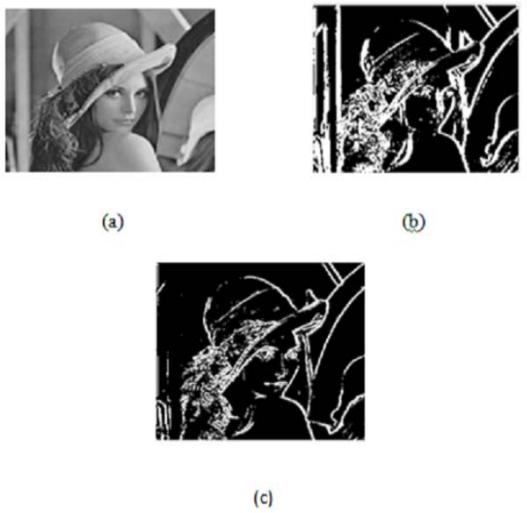


Fig.11: a) Original Image b) XSG based edge detection (Sobel) c) FPGA based edge detection (Sobel)

Results of edge detection using Prewitt operator for XSG and FPGA based implementation is shown in Fig.12

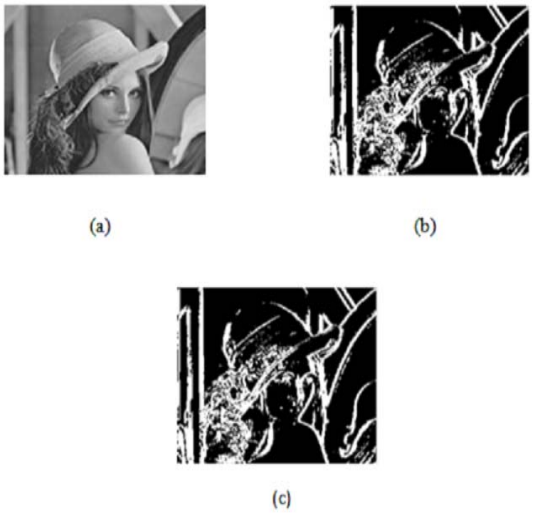


Fig.12: a) Original Image b) XSG based edge detection (Prewitt) c) FPGA based edge detection (Prewitt)

Table 1 shows comparative analysis of the resource utilization of Spartan-3E board. Summary is depicted in the table shown. The proposed approach is multiplier free so it optimized area and power resource.

Table 1: Comparison of device utilization summary

| Comparison of device utilization summary | | |
|---|---|---|
| **Logic Utilization** | **Sobel operator** | **Prewitt operator** |
| Number of slice flip flops | 448 / 9,312 | 51 / 9,312 |
| Number of 4 input LUTs | 472 / 9,312 | 97 / 9,312 |
| Number of occupied slices | 385 / 4,656 | 8/4,656 |
| Number of slices (only related logic) | 385 / 385 | 39/385 |
| Number of slices (only unrelated logic) | 0 / 385 | 1/385 |
| Total number of 4 input LUTs | 472 / 9,312 | 470/9,312 |

Table 2 shows comparative analysis total power dissipation using sobel and prewitt operator. Total power includes static (Quiescent power) and dynamic power. It also depicts comparative analysis of the minimum time period and maximum operating frequency.

Table 2: Comparison of Power dissipation and Maximum frequency

| **Operator** | **Total power (W)** | **Min period (Max frequency)** |
|---|---|---|
| Sobel | 0.181 W | 3.461 ns (288.934 MHz) |
| Prewitt | 0.182 W | 5.753 ns (173.822 MHz) |

## V. CONCLUSION

In this paper sobel and prewitt edge detection algorithm is implementation over Spartan-3E FPGA platform. Edges are the significant features for image processing and many computer vision applications. For real time applications edge detection algorithm has to be implemented over hardware platform. Sobel algorithm is better suited for real time applications over its contemporary prewitt algorithm, owing to its optimized power and area constraint. Maximum operating frequency for sobel architecture is greater than prewitt architecture. FPGA has high speed multipliers, parallel architecture which makes them superior over their DSP counterparts. It offers short 'Turn Around Time' (TAT) and small 'Non Recurrent Expense' (NRE). 'Xilinx System Generator' tool of Matlab provides an efficient and simplified approach hardware implementation (FPGA).

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## AUTHOR BIOGRAPH

***Swapnil G. Kavitkar*** completed B.Tech. in Electronics and Telecommunication Engineering from Government College of Engineering Amravati, India in 2011 and now pursuing M.Tech with specialization Electronics Systems and Communication from Government college of Engineering Amravati. He has published review paper on image processing in IJESRT. His area of research includes image processing, Digital Signal Processing, and Embedded system.

***P. L. Paikrao*** received the B.E. degree in Industrial Electronics from Dr. BAM University, Aurangabad in 2003 and the M. Tech. degree in Electronics from SGGSIE&T, Nanded in 2006. He is working as Assistant Professor, Electronics and Telecommunication Engineering Department, Government College of Engineering Amravati. He has attended An International Workshop on Global ICT Standardization Forum for India (AICTE Delhi & CTIF International Journal of Innovative Technology and Exploring Engineering (IJITEE) ISSN: 2278-3075, Volume-2, Issue-4, March, 2013 (Denmark) at Sinhgadh Institute of Technology, Lonawala, Pune and a workshop on ECG Analysis and Interpretation conducted by Prof. P. W. Macfarlane, Glasgow, Scotland. He has recently published the papers in conference on „Filtering Audio Signal by using Blackfin BF533EZ kit lite evaluation board and visual DSP++ and „Project Aura: Towards Acquiescent Pervasive Computing" in National Level Technical Colloquium "Technozest-2K11", at AVCOE, Sangamner.